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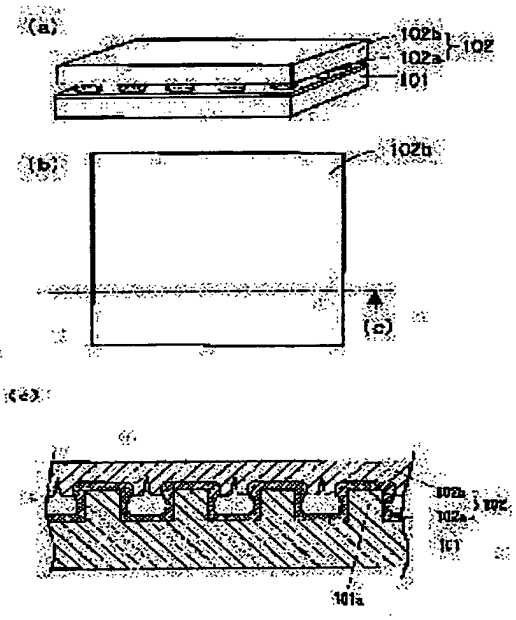
(54) METHOD FOR PRODUCING SEMICONDUCTOR CRYSTAL AND SEMICONDUCTOR LIGHT EMITTING ELEMENT

(57)Abstract:
PROBLEM TO BE SOLVED: To obtain a high quality semiconductor crystal nearly free from dislocations.
SOLUTION: When a substrate layer (a desired semiconductor crystal) of a group III nitride-based compound is grown on a ground substrate having a plurality of projection parts, cavities where no semiconductor crystal is deposited are formed at each of spaces between the projected parts, depending on the size of each projected part, the distance between the projected parts, crystal growth conditions, or the like. Therefore, when the thickness of the substrate layer is made sufficiently larger than the height of the projected parts, an internal stress or an external stress tends to act on the projected parts in a concentrated manner. These stresses act especially on the projected parts as the shear stress, and when the stresses become large enough, fracture occurs at the projected parts. Accordingly, it becomes possible to easily separate the ground substrate and the substrate layer by the use of these stresses and to obtain the semiconductor crystal independent from the ground substrate. The stresses are more easily concentrated on the projected parts as the sizes of the cavities become larger, and it becomes possible to separate the substrate layer from the ground substrate without failure.



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* NOTICES *

1. This document has been translated by computer.So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
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CLAIMS

[Claim(s)]
[Claim 1] The manufacture method of a semiconducting crystal characterized by providing the following A longitudinal direction crystal-growth operation is used and it is on a ground substrate. Height formation process which is the method of obtaining the semiconducting crystal which became independent of the aforementioned ground substrate by forming the substrate layer which consists of an III group nitride system compound semiconductor, and forms many heights on the aforemention d ground substrate. The crystal-growth process to which the crystal growth of the aforementioned substrate layer is carried out until this growth side is mutually connected respectively as first growth side where the aforementioned substrate layer starts a crystal growth and it grows up to be a series of abbreviation flat surfaces at least in a part of front face [at least] of the aforementioned h ight. The partition stage which separates the aforementioned substrate layer and the aforementioned ground substrate by fracturing the aforementioned height.
[Claim 2] The manufacture method of the semiconducting crystal according to claim 1 charact rized by generating the stress based on the coefficient-of-thermal-expansion difference of the aforementioned substrate layer and the aforementioned ground substrate, and fracturing the aforementioned h ight by cooling or heating the aforementioned substrate layer and the aforementioned ground substrate using this stress.
[Claim 3] A longitudinal direction crystal-growth operation is used and it is on a ground substrate. By forming the substrate layer which consists of an III group nitride system compound semiconductor The height formation process which is the method of obtaining a semiconducting crystal and forms many heights on the aforementioned ground substrate, A part of front face [at least] of the aforementioned height until this growth side is connected mutually respectively and it grows up to be a series of abbreviation flat surfaces at least as first growth side where the aforementioned substrate layer starts crystal growth Have the crystal-growth process to which the crystal growth of the aforementioned substrate layer is carried out, and it sets at the aforementioned crystal-growth process. Above By adjusting the amount q of feeding of an III group nitride system compound semiconductor The manufacture method of the semiconducting crystal characterized by controlling the difference (b-a) of the rate of crystal growth a of the aforementioned III group nitride system compound semiconductor in some [at least] exposed regions of the trough between the aforementioned heights of the aforementioned ground substrate, and the rate of crystal growth b in the parietal region of the aforementioned height to abbreviation maximum.
[Claim 4] It describes above in the aforementioned crystal-growth process. The claim 1 characterized by controlling the difference (b-a) of the rate of crystal growth a of the aforementioned III group nitride system compound semiconductor in some [at least] exposed regions of the trough between the aforementioned heights of the aforementioned ground substrate, and the rate of crystal growth b in the parietal region of the aforementioned height to abbreviation maximum by adjusting the amount q of feeding of an III group nitride system compound semiconductor, or the manufacture method of a semiconducting crystal according to claim 2.
[Claim 5] They are 1micromol / min about the aforementioned amount q of feeding. They are 100micromol / min above. The claim 3 characterized by considering as the following, or the manufacture method of a semiconducting crystal according to claim 4.
[Claim 6] The manufacture method of a semiconducting crystal given in any 1 term of the claim 1 characterized by using silicon (Si) or carbonization silicon (SiC) as a material of the aforementioned ground substrate, or a claim 5.

[Claim 7]. The manufacture method of a semiconducting crystal given in any 1 term of the claim 1 characterized by forming the aforementioned height in the aforementioned height formation process, using Si (111) as a material of the aforementioned ground substrate so that Si (111) side may not be exposed to the exposed region of the trough between the aforementioned heights of the aforementioned ground substrate, or a claim 6.

[Claim 8] The manufacture method of a semiconducting crystal given in any 1 term of the claim 1 characterized by having the process which forms in the front face of the aforementioned height at least the buffer layer which consists of "Alx Ga1−x N (0< x<=1)" after the aforementioned height formation process, or a claim 7.

[Claim 9] The manufacture method of the semiconducting crystal according to claim 8 characterized by forming the thickness of the aforementioned buffer layer below in the lengthwise height of the aforementioned height.

[Claim 10] The manufacture method of a semiconducting crystal given in any 1 term of the claim 1 characterized by setting thickness of the aforementioned substrate layer to 50 micrometers or more in the aforementioned crystal−growth process, or a claim 9.

[Claim 11] The manufacture method of a semiconducting crystal given in any 1 term of the claim 1 characterized by changing a crystal−growth method into the quick crystal−growth method of the rate of crystal growth on the way from the late crystal−growth method of the rate of crystal growth in the aforementioned crystal−growth process, or a claim 10.

[Claim 12] The manufacture method of a semiconducting crystal given in any 1 term of the claim 1 characterized by forming the aforementioned height in the aforementioned height formation process so that the aforementioned height may be arranged abbreviation regular intervals or an abbreviation fixed period, or a claim 11.

[Claim 13] The manufacture method of the semiconducting crystal according to claim 12 characterized by forming the aforementioned height in the aforementioned height formation process on the lattice point of the two−dimensional triangular grid to which one side makes the keynote the abbreviation equilateral triangle of 0.1 micrometers or more.

[Claim 14] The manufacture method of a semiconducting crystal given in any 1 term of the claim 1 characterized by forming the horizontal section configuration of the aforementioned height in an abbreviation equilateral triangle, an approximate regular hexagon, an approximate circle form, or a square in the aforementioned height formation process, or a claim 13.

[Claim 15] The manufacture method of a semiconducting crystal given in any 1 term of the claim 1 characterized by setting the arrangement interval of the aforementioned height to 0.1 micrometers or more and 10 micrometers or less in the aforementioned height formation process, or a claim 14.

[Claim 16] The manufacture method of a semiconducting crystal given in any 1 term of the claim 1 characterized by setting the lengthwise height of the aforementioned height to 0.5 micrometers or more and 20 micrometers or less in the aforementioned height formation process, or a claim 15.

[Claim 17] The manufacture method of a semiconducting crystal given in any 1 term of the claim 1 characterized by setting the size of the longitudinal direction of the aforementioned height, width of face, or a diameter to 0.1 micrometers or more and 10 micrometers or less in the aforementioned height formation process, or a claim 16.

[Claim 18] Before the aforementioned crystal−growth process, by physical processing of optical processing, such as various etching, electron−beam−irradiation processing, and laser, chemical preparation or cutting, polish, etc. By deteriorating or changing the crystallinity of some [at least] exposed regions of the trough between the aforementioned heights of the aforementioned ground substrate, or the molecular structure The above in the aforementioned exposed region The manufacture method of a semiconducting crystal given in any 1 term of the claim 1 characterized by reducing the rate of crystal growth a of an III group nitride system compound semiconductor, or a claim 17.

[Claim 19] In the state [leaving the substrate which consists of the aforementioned ground substrate and the aforementioned substrate layer to the reaction chamber of growth equipment in the aforementioned partition stage, and having passed the ammonia (NH3) gas of abbreviation constant flow to the aforementioned reaction chamber] The manufacture method of a semiconducting crystal given in any 1 term of the claim 1 characterized by cooling the aforementioned substrate to abbreviation ordinary temperature with the cooling rate about "−100 degree−C/min−−0.5 degree C/min" in general, a claim 2, a claim 4, or a claim 18.

[Claim 20] The manufacture method of a semiconducting crystal given in any 1 term of the claim 1 characterized by having the wreckage removal process that chemical or physical processing processing

of etching etc. removes at least the fracture wreckage of the aforementioned height which remained a the rear face of the aforementioned substrate layer after the aforementioned partition stage, a claim 2 a claim 4, or a claim 19.

[Claim 21] It is characterized by having the aforementioned semiconducting crystal manufactured by any 1 term of a claim 1 or a claim 20 using the manufacture method of the semiconducting crystal a publication as a crystal-growth substrate. III group nitride system compound semiconductor light emitting device.

[Claim 22] It is characterized by what was manufactured by the crystal growth which used as the crystal-growth substrate the aforementioned semiconducting crystal manufactured by any 1 term of a claim 1 or a claim 20 using the manufacture method of the semiconducting crystal a publication. III group nitride system compound semiconductor light emitting device.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention uses a longitudinal direction crystal-growth operation, and is on a ground substrate. It is related with the manufacture method of a semiconducting crystal of obtaining a crystal-growth substrate, by forming the substrate lay r which consists of an III group nitride system compound semiconductor.
[0002]
[Description of the Prior Art] If the crystal growth of the nitride semiconductors, such as a gallium nitride (GaN), is carried out on the ground substrate which consists of silicon (Si) etc. and it cools to ordinary temperature after that so that it may illustrate to drawing 5 for example, generally it is known that many transposition and cracks will go into a nitride semiconductor layer.
[0003]
[Problem(s) to be Solved by the Invention] Thus, when many transposition and cracks went into the growth phase (nitride semiconductor layer) and a device is produced on it, it becomes the cause which brings a result which many a lattice defect, transposition, deformation, cracks, etc. produce, and causes degradation of a device property into a device. Moreover, the ground substrate which consists, for example of silicon (Si) etc. is removed, and when it is going to leave only a growth phase and is going to obtain the independent substrate (crystal), the thing of a large area (more than 1cm2) is not obtained by operation of the above-mentioned transposition, a crack, etc.
[0004] It is that accomplish this invention in order to solve the above-mentioned technical problem, and the purpose does not have a crack, and the density of transposition obtains the semiconducting crystal (crystal-growth substrate) of low high quality.
[0005]
[A The means for solving a technical problem, an operation, and an effect of the invention] The following meanses are effective in order to solve the above-mentioned technical problem. Namely, the 1st means uses a longitudinal direction crystal-growth operation, and is on a ground substrate. In the manufacturing process which obtains the semiconducting crystal which became independent of a ground substrate by forming the substrate layer which consists of an III group nitride system compound semiconductor The crystal-growth process to which the crystal growth of the substrate layer is carried out until this growth side is mutually connected with the height formation process which forms many heights on a ground substrate respectively in a part of front face [at least] of this height as first growth side where a substrate layer starts a crystal growth and it grows up to be a series of abbreviation flat surfaces at least, It is preparing the partition stage which separates a substrate layer and a ground substrate by fracturing a height.
[0006] however, to general "III group nitride system compound semiconductor" said here The semiconductor of the arbitrary mixed-crystal ratios expressed with 2 yuan, 3 yuan, or 4 yuan the general formula which "Alx Gay In (1-x-y) N (0<=x<=1, 0<=y<=1, 0 <=x+y<=1) N" Changes is contained. Furthermore, also let the semiconductor with which p type or the n type impurity was added be the criteria of the "III group nitride system compound semiconductor" of this specification. Moreover, the above Let the semiconductor which replaced the part of the III group elements (aluminum, Ga, In) with boron (B), the thallium (Tl), etc., or replaced some nitrogen (N) by Lynn (P), arsenic (As), antimony (Sb), the bismuth (Bi), etc. be the criteria of the "III group nitride system compound semiconductor" of this specification. moreover -- as the impurity of the above-mentioned p type -- magnesium (Mg) -- or calcium (calcium) etc. can be added Moreover, as an impurity of the above-mentioned n type, silicon

(Si), sulfur (S), a selenium (Se), a tellurium (Te) or germanium (germanium), etc. can be added, for example. Moreover, these impurities may add two or more elements simultaneously, and may add both molds (p type and n type) simultaneously.

[0007] For example, on the ground substrate which has many heights so that it may illustrate to drawi 1 When growing up the substrate layer (semiconducting crystal) which consists of an III group nitride system compound, formation of the "cavity" by which a laminating is not carried out of a semiconducting crystal is attained between each height (side of a height) by adjusting the size and arrangement interval of a height, crystal-growth terms and conditions, etc. For this reason, if substrate layer thickness is enlarged enough as compared with the height of a height, internal stress or external stress will become easy to act on this height intensively. When it acts as shearing stress to a height etc. and this stress becomes large, a height fractures the result, especially such stress. Therefore, if this stress is used, it will become possible to separate a ground substrate and a substrate layer easily (ablation). By this means, the crystal (substrate layer) which became independent of a ground substrat can be obtained. Moreover, it becomes easy to concentrate stress (shearing stress) on a height, so tha the above-mentioned "cavity" is formed greatly.

[0008] moreover -- for example, the distortion based on [since the contact part of a ground substrate and a substrate layer (or desired semiconducting-crystal layer) is narrowly limited by forming the above heights so that drawing 1 may also show] both lattice constant difference -- being generated -- being hard -- "the stress based on the lattice constant difference between a ground substrate and a substrate layer" is eased For this reason, in case a substrate layer (desired semiconducting crystal) carries out a crystal growth, the unnecessary stress committed in the substrate layer under growth is suppressed, and the generating density of transposition or a crack is reduced.

[0009] In addition, in case a ground substrate and a substrate layer are separated (ablation), a part of substrate layer may remain in a ground substrate side, or a part of ground substrate (example : fracture wreckage of a height) may remain in a substrate layer side. Namely, the above-mentioned partition stag is not premised on perfect separation of each material which makes some wreckage of such material there be nothing (requirement).

[0010] Moreover, 2nd means to solve the above-mentioned technical problem is generating the stress based on the coefficient-of-thermal-expansion difference of a substrate layer and a ground substrate, and fracturing the above-mentioned height using this stress by setting for these 1st means, and cooling or heating a substrate layer and a ground substrate. According to this means, it becomes possible to generate the above-mentioned stress easily.

[0011] Moreover, the 3rd means uses a longitudinal direction crystal-growth operation, and is on a ground substrate. In the manufacturing process which obtains a semiconducting crystal by forming the substrate layer which consists of an III group nitride system compound semiconductor The crystal-growth process to which the crystal growth of the substrate layer is carried out until this growth side is mutually connected with the height formation process which forms many heights on a ground substrate respectively in a part of front face [at least] of this height as first growth side where a substrate layer starts a crystal growth and it grows up to be a series of abbreviation flat surfaces at least is established. In this crystal-growth process By adjusting the amount q of feeding of an III group nitride system compound semiconductor It can set to some [at least] exposed regions of the trough between the heights of a ground substrate. It is controlling the difference (b-a) of the rate of crystal growth a of an III group nitride system compound semiconductor, and the rate of crystal growth b in the parietal region of a height to abbreviation maximum.

[0012] According to this means, the rate of crystal growth near the parietal region of a height becomes large relatively, and the crystal growth near [above] an exposed region is suppressed comparatively, and becomes dominant [the crystal growth from near the parietal region]. Consequently, longitudinal direction growth (ELO) of the substrate layer started from near the parietal region of a height becomes remarkable, and "the stress based on the lattice constant difference between a ground substrate and a substrate layer" committed in a substrate layer at the time of the crystal growth of a substrate layer is eased. Therefore, the crystal structure of a substrate layer is stabilized and it is hard coming to generate transposition and a crack in a substrate layer. Moreover, if longitudinal direction growth (ELO) of a substrate layer becomes remarkable, a comparatively big cavity may be made in the side (between each height) of a height, for example.

[0013] For example, when irregularity is formed on the front face of a ground substrate a suitable size, an interval, or a period so that it may illustrate to drawing 1 , generally except the periphery part near the periphery side attachment wall of a ground substrate, the direction of the amount of supply per the

unit time and unit area of crystal material of a crevice (trough) tends to decrease compared with near the upper surface of heights (height). This inclination becomes possible [controlling the above-mentioned difference (b-a) to abbreviation maximum] by controlling these terms and conditions the optimal or suitably, although it depends in the flow rate of the gas stream of crystal material, temperature, the direction, etc.

[0014] Moreover, the 4th means can be set in the above 1st or the crystal-growth process of the 2nd means to some [at least] exposed regions of the trough between the heights of a ground substrate b adjusting the amount q of feeding of an III group nitride system compound semiconductor. It is controlling the difference (b-a) of the rate of crystal growth a of an III group nitride system compound semiconductor, and the rate of crystal growth b in the parietal region of a height to abbreviation maximum.

[0015] Also in this case, "the stress based on the lattice constant difference between a ground substrate and a substrate layer" committed in a substrate layer at the time of the crystal growth of a substrate layer is eased like the above-mentioned means, the crystal structure of a substrate layer is stabilized, and it is hard coming to generate transposition and a crack in a substrate layer. When longitudinal direction growth is remarkable, it becomes comparatively remarkable, so that a cavity is made by this operation and effect between each height (side of a height). Moreover, if a cavity is forme in the side (between each height) of a height, it will become easy to concentrate shearing stress on a height, and shearing stress will become easy to separate a ground substrate and a substrate layer in th above-mentioned partition stage. This operation and effect become remarkable, so that the cavity between each height (side of a height) becomes large.

[0016] Moreover, it sets for the above 3rd or the 4th means, and the 5th means is 1micromol / min about the above-mentioned amount q of feeding. They are 100micromol / min above. It is considering a the following.

[0017] The more desirable above-mentioned amount q of feeding is 5micromol / min. They are 90micromol / min above. The following is good. Furthermore, although it depends also on terms and conditions, such as specification of ground substrates, such as a size of the height formed, and a form, an arrangement interval, a kind of feed, and the direction of feeder current, a crystal-growth method, as a desirable value, they are 10-80micromol / min in general. A grade is ideal. Since it will become difficul to control the above-mentioned difference (b-a) to abbreviation maximum if this value is too large, it becomes difficult to form a big cavity between each height (side of a height). As for the crystallinity of the single crystal of a substrate layer, it becomes easy to deteriorate and is not desirable to follow, in such a case for the stress in the crystal based on a lattice constant difference comparatively to be har to be eased, and for transposition to occur etc.

[0018] moreover, the time of stress (shearing stress) separating a ground substrate and a substrate layer — a height — if there is no cavity of the side or this cavity is small — a height — stress — concentrating — being hard — fracture of a height is hard coming to happen and is not desirable On the other hand, if the amount q of feeding is too small, crystal-growth time will be taken too much and i will become disadvantageous in respect of productivity, and it is not desirable.

[0019] Moreover, the 6th means is using silicon (Si) or carbonization silicon (SiC) as a material of a ground substrate in any the above 1st or 5th one means. moreover -- as the material of other ground substrates — GaN, AlN, GaAs, InP, GaP, MgO and ZnO, and MgAl 2O4 etc. -- it is useful and sapphire, a spinel, manganese oxide, an oxidization gallium lithium (LiGaO2), a molybdenum sulfide (MoS), etc. are usable However, when separating a ground substrate and a substrate layer using the shearing stress based on a coefficient-of-thermal-expansion difference, it is desirable to choose the combination to which the coefficient-of-thermal-expansion difference between both material does not become small, and it is desirable to choose as a ground substrate side the material to which fracture tends to take place.

[0020] Moreover, the 7th means is forming a height, using Si (111) as a material of a ground substrate, so that Si (111) side's may not be exposed to the exposed region of the trough between the heights of a ground substrate in a height formation process in any the above 1st or 6th one means. According to this means, since the rate of crystal growth a of the exposed surface of the above-mentioned trough can be suppressed small, it becomes possible to carry out the abbreviation maximization of the above-mentioned difference (b-a) stably, with crystallinity maintained.

[0021] Moreover, the means of the octavus is establishing the process which forms the buffer layer which consists of "Alx Ga1-x N (0< x<=1)" on the surface of a height at least after the height formation process of any the above 1st or 7th one means.

[0022] however, the buffer layer of another further the above [buffer layer / above-mentioned] and the interlayer of **** composition (example : AlN and AlGaN) -- other periodic or layers and alternati -- or you may carry out a laminating so that multilayer structure may be constituted
[0023] The same operation principle as the former of being able to ease the stress committed in the substrate layer (growth phase) resulting from a lattice constant difference by the laminating of such a buffer layer (or interlayer) enables it to raise crystallinity.
[0024] Moreover, the 9th means is forming the thickness of a buffer layer below in the lengthwise heig of a height in the means of the above-mentioned octavus. Moreover, as an absolute standard, th thickness of a buffer layer has about 0.01 micrometers or more and desirable 1 micrometer or l ss. By this means, only the crystal layer (example : GaN layer) of the request formed on a buffer layer can be grown up into a longitudinal direction good. That is, "the stress based on a lattice constant difference" applied to the crystal layer formed on a buffer layer at the time of a crystal growth is mitigated by this means, and dislocation density can decrease effectively by it.
[0025] According to the above-mentioned means [like] but which has the direction of GaN which is easy to be formed all over the abbreviation for the front face which the ground substrate exposed, and forms a desired crystal-growth layer etc. originally in the inclination which is easy to carry out longitudinal direction growth from AlN, AlGaN, etc., AlN which forms a buffer layer etc., AlGaN, etc. can form more certainly big a "cavity" in the side of a height.
[0026] Moreover, when a substrate layer is separated from a ground substrate, a crystal layer (layer of the request formed on a buffer layer) is broadly exposed also to the rear face (field of a side with the ground substrate) of a substrate layer soon with this means. Therefore, in case an electrode is form d in the rear face of a substrate layer, it becomes easy to suppress electric resistance.
[0027] In addition, the thickness of a buffer layer has 0.1 micrometers or more and good 0.5 micrometers or less more desirably, although about 0.01 micrometers - about 1 micrometer is as above mentioned a in general appropriate range. A cavity becomes easy to become small and is not desirable this thickness is too thick. Moreover, if this thickness is made thin too much, it will become difficult to form a buffer layer to abbreviation homogeneity. If the membrane formation nonuniformity (part which is not fully formed) of a buffer layer arises in near the upper part of a height especially, it becomes easy t produce nonuniformity also in crystallinity, and is not desirable.
[0028] Moreover, the 10th means is setting thickness of a substrate layer to 50 micrometers or more ir the above 1st or the crystal-growth process of any 9th one means.
[0029] The tensile stress to a substrate layer is eased and the thickness of the substrate layer (III group nitride system compound semiconductor) which carries out a crystal growth can decrease the generating density of the transposition of a substrate layer, or a crack, so that about 50 micrometers or more are desirable and this thickness is thick. Furthermore, a substrate layer can be strengthened simultaneously and it becomes that it is easy to centralize the above-mentioned shearing stress on the above-mentioned height.
[0030] Moreover, the 11th means is changing a crystal-growth method into the quick crystal-growth method of the rate of crystal growth on the way from the late crystal-growth method of the rate of crystal growth in the above 1st or the crystal-growth process of any 10th one means.
[0031] For example, if the crystal-growth method (example : the MOVPE method) which is easy to make the above-mentioned difference (b-a) the abbreviation maximum is adopted and setting thickness to 50 micrometers or more efficiently after that adopts an easy crystal-growth method (example : the HVPE method) until a crystal-growth side grows into a series of abbreviation planes, it will become possible to obtain a crystalline good semiconducting crystal for a short time.
[0032] Moreover, the 12th means is forming the above-mentioned height so that a height's may be arranged abbreviation regular intervals or an abbreviation fixed period in the height formation process of any the above 1st or 11th one means.
[0033] Thereby, it becomes equal on the whole omitting the growth conditions of longitudinal direction growth, and it is hard coming to generate nonuniformity in a crystalline quality. moreover, the crystal-growth method the late crystal-growth method of the rate of crystal growth to the rate of crystal growth is quick since it is hard coming to generate local variation at time until the upper part of the trough between heights is completely covered by the substrate layer -- on the way -- the case where come out and a crystal-growth method is changed -- the time -- exact -- an early stage -- or it becomes easy it to be decided for that it will be a meaning Moreover, by this means, since the above-mentioned cavity serves as a size with an equal abbreviation respectively and becomes possible [distributing the above-mentioned shearing stress to each height equally / abbreviation], fracture of all

heights arises without nonuniformity and separation with a ground substrate and a substrate layer can carry out certainly.

[0034] Moreover, the 13th means is forming a height on the lattice point of the two-dimensional triangular grid to which one side's makes the keynote the abbreviation equilateral triangle of 0.1 micrometers or more in the height formation process of the 12th above-mentioned means. By this means, the 12th above-mentioned means can be carried out correctly and certainly more concretely, and, therefore, the number of transposition can be reduced certainly.

[0035] Moreover, the 14th means is forming the horizontal section configuration of a height in an abbreviation equilateral triangle, an approximate regular hexagon, an approximate circle form, or a squai in the height formation process of any the above 1st or 13th one means. the direction of the crystallographic axis of the crystal formed from an III group nitride system compound semiconductor of this means -- each part -- a set -- easy -- arbitrary horizontal directions since it becomes -- receiving -- length with a horizontal height (size) -- abbreviation -- since it can restrict uniformly, the number of transposition can be suppressed Since especially a right hexagon and an equilateral triangle tend to agree with the crystal structure of a semiconducting crystal, they are more desirable. Moreover a round shape and a square have the merit compared with the present condition of the present general processing technical level referred to as being easy to form in respect of a manufacturing technology.

[0036] Moreover, the 15th means is setting the arrangement interval (arrangement period) of a height t 0.1 micrometers or more and 10 micrometers or less in the height formation process of any th above 1st or 14th one means. More desirably, although it is dependent also on the operation conditions of a crystal growth, the arrangement interval of a height has good about 0.5-8 micrometers. However, this arrangement interval means the distance between the central point of each height which approaches mutually.

[0037] While this means enables it to cover the upper part of the trough of a height in a substrate layer it becomes possible to form a cavity between heights. If this value is too small, an operation of ELO will no longer be obtained hardly and crystallinity will deteriorate. Unless the cavity formed becomes small too much and makes thickness of a substrate layer larger than required, it becomes moreover, less eas to fracture a height.

[0038] Moreover, if this value becomes large too much, it will become impossible to cover the upper par of the trough of a height in a substrate layer certainly, and a crystal (substrate layer) homogeneous [crystallinity] and good will no longer be obtained. If this value is still too larger, since the exposed surface of a trough will become vast too much, and an operation of ELO will hardly be obtained no longer and a cavity will no longer be formed at all, unless crystallinity deteriorates and thickness of a substrate layer is made larger than required, it becomes or less easy to fracture a height.

[0039] Moreover, the 16th means is setting the lengthwise height of a height to 0.5 micrometers or mor and 20 micrometers or less in the height formation process of any the above 1st or 15th one means. More desirably, although it is dependent also on the operation conditions of a crystal growth, the lengthwise height of a height has good about 0.8-5 micrometers. If this height is too short, like the case where there is no height, an operation of ELO will no longer be obtained hardly and crystallinity will deteriorate. Moreover, if this height is too short, the above-mentioned cavity will no longer be formed. Moreover, if this height is too high, the formation of a height itself becomes difficult, formation of a height takes time more than required, or material of a ground substrate is consumed more than required and it is not desirable. Moreover, if this height is too high, it will become difficult for lengthwise [of a height] to distribute and for shearing stress to make a height fracture certainly.

[0040] Moreover, the 17th means is setting the size of the longitudinal direction of a height, width of face, or a diameter to 0.1 micrometers or more and 10 micrometers or less in the height formation process of any the above 1st or 16th one means. More desirably, although it is dependent also on the operation conditions of a crystal growth, the size of the longitudinal direction of a height, width of face, or a diameter has good about 0.5-5 micrometers. If this size is too thick, the influence of stress which works in a substrate layer (growth phase) based on a lattice constant difference will become large, and it will become easy to increase the number of dislocation of a substrate layer. Moreover, if too thin, the own formation of a height becomes difficult, or the rate of crystal growth b of the parietal region of a height becomes slow, and it is not desirable.

[0041] Moreover, if the size of the longitudinal direction of a height, width of face, or a diameter is too large in case a height is made to fracture with stress (shearing stress etc.), it becomes easy to produce the portion which is not fractured certainly, and is not desirable. Moreover, the size of the influence of stress which works in a substrate layer (growth phase) based on a lattice constant difference does not

depend only on the size (length) of the longitudinal direction of a height, and is dependent on the arrangement interval of a height etc. And if these setting ranges are unsuitable, the influence of stress based on a lattice constant difference becomes large as mentioned above, and it becomes easy to increase the number of dislocation of a substrate layer, and is not desirable.

[0042] Moreover, since there is an optimum value or a proper range in the size of the longitudinal direction near the parietal region of a height, width of face, or a diameter as mentioned above, the configuration of the upper surface of a height, a base, or a horizontal section has the configuration (the shape of an island) closed locally at least, and the configuration still better for it closed to convex toward the outside, and the configuration of this upper surface, a base, or a horizontal section has an approximate circle form, an abbreviation regular polygon good for it, etc. By such setup, it becomes eas certainly to arbitrary horizontal directions to realize an above-mentioned optimum value or the above-mentioned proper range.

[0043] Moreover, the 18th means is set for any the above 1st or 17th one means. Before a crystal-growth process, by physical processing of optical processing, such as various etching, electron-beam-irradiation processing, and laser, chemical preparation or cutting, polish, etc. By deteriorating or changing the crystallinity of some [at least] exposed regions of the trough between the heights of a ground substrate, or the molecular structure, it can set to this exposed region. It is reducing the rate o crystal growth a of an III group nitride system compound semiconductor. By this means, difference (b-a of the aforementioned rate of crystal growth can be enlarged more. Therefore, according to this means, since the rate of crystal growth near the parietal region of a height becomes large relatively, "the stres based on the lattice constant difference between a ground substrate and a substrate layer" committed in a substrate layer at the time of the crystal growth of a substrate layer is eased by the same operation as the above, and it is hard coming to generate dislocation and a crack in a substrate layer.

[0044] Moreover, in any one above-mentioned partition stage, the 19th means is in a state [leaving the substrate which consists of a ground substrate and a substrate layer to the reaction chamber of growth equipment, and having passed the ammonia (NH3) gas of abbreviation constant flow to the reaction chamber], and is cooling a substrate to abbreviation ordinary temperature with the cooling rate about "-100 degree-C/min--0.5 degree C/min" in general. For example, the aforementioned partition stage can be carried out by such means, maintaining the crystallinity of a substrate layer good.

[0045] Moreover, the 20th means is establishing at least the wreckage removal process chemical or physical processing processing of etching etc. removing the fracture wreckage of the height which remained in the rear face of a substrate layer, after any one above-mentioned partition stage. the current nonuniformity and the electric resistance which are produced near the interface of an electrode and a substrate layer when electrodes, such as a semiconductor light emitting device, are formed in the rear face (field of the side which made the ground substrate exfoliate) of a substrate layer according to this means — it can suppress — therefore — reduction of driver voltage — or improvement in luminescence intensity etc. can be aimed at

[0046] Furthermore, since the absorption of light near a mirror plane and dispersion are reduced and a reflection factor improves in case an electrode is used also as reflecting mirrors, such as a semiconductor light emitting device, by removing the fracture wreckage of a height, luminescence intensity improves. Moreover, since even the buffer layer of the rear face of a substrate layer can be removed or the flatness of the rear face of a substrate layer can also be improved when this wreckage removal process is carried out by physical processing processing of polish etc. for example, the above-mentioned operation effects, such as suppression of current nonuniformity or electric resistance, or the absorption of light near a mirror plane, reduction of dispersion, can be reinforced further.

[0047] Moreover, in the 21st means and an III group nitride system compound semiconductor light emitting device, it is having the semiconducting crystal manufactured using the manufacture method of the semiconducting crystal which depends on any the above 1st or 20th one means as a crystal-growth substrate. According to this means, it becomes crystallinity is good and more possible [manufacturing an III group nitride system compound semiconductor light emitting device] than a semiconductor with little internal stress, or easy.

[0048] Moreover, the 22nd means is manufacturing an III group nitride system compound semiconductor light emitting device by the crystal growth which used as the crystal-growth substrate the semiconducting crystal manufactured using the manufacture method of the semiconducting crystal which depends on any the above 1st or 20th one means. According to this means, it becomes crystallinity is good and more possible [manufacturing an III group nitride system compound semiconductor light emitting device] than a semiconductor with little internal stress, or easy. The

aforementioned technical problem is solvable with the above means.
[0049]
[Embodiments of the Invention] Hereafter, this invention is explained based on a concrete example. However, this invention is not limited to the example shown below. Hereafter, the outline of the manufacture procedure of the semiconducting crystal (crystal-growth substrate) in the example of this invention is illustrated.
[0050] [1] As shown in the height formation process drawing 2, height 101a of the shape of an approximate circle pilaster with a diameter [of about 1 micrometer] and a height of about 1 micromet was formed at intervals of about 2-micrometer arrangement by the dry etching using photo lithography on Si (111) side of the ground substrate 101 of the single crystal which consists of silicon. Height 101a was formed so that the center at the base of a pillar of height 101a might be arranged on each lattice point of the two-dimensional triangular grid which makes the keynote the abbreviation equilateral triangle whose one side is about 2 micrometers as an array form. However, thickness of th ground substrate 101 was set to about 200 micrometers.
[0051] [2] At the crystal-growth process book crystal-growth process, as shown in drawing 4 , the growth process until a crystal-growth side is mutually connected respectively from the upper surface (initial state) of height 101a and grows up to be a series of abbreviation planes was carried out according to the organometallic compound vapor growth (the MOVPE method), and the growth process until it grows up to be the thick film this substrate layer (crystal layer) of whose is about 200 micrometers after that was carried out according to the hydride vapor growth (the HVPE method). In addition, at this crystal-growth process, it is ammonia (NH3). Gas, carrier gas (H2, N2), trimethylgallium (Ga3 (CH3)) gas (it is described as "TMG" below), and trimethylaluminum (aluminum3 (CH3)) gas (it is described as "TMA" below) were used.
[0052] (a) Organic washing and acid treatment washed first the ground substrate 101 (drawing 2) in which the above-mentioned height 101a was prepared, the susceptor laid in the reaction chamber of crystal-growth equipment was equipped, and the ground substrate 101 was baked at the temperatur o 1100 degrees C, passing H2 to a reaction chamber by the ordinary pressure.
[0053] (b) Next, according to the MOVPE method, H2, and NH3, TMG and TMA were supplied on the above-mentioned ground substrate 101, and AlGaN buffer-layer (one layer of substrate ****) 102a was formed. The crystal-growth temperature of this AlGaN buffer-layer 102a was about 1100 degrees C, and thickness was about 0.3 micrometers. (Drawing 3)
(c) On this AlGaN buffer-layer (one layer of substrate ****) 102a, it is GaN layer 102b of two layer of about 5 micrometers of a part of substrate ****, i.e., thickness, H2 and NH3 And TMG was supplied and the crystal growth was carried out at the growth temperature of 1075 degrees C. According to this process, as shown in drawing 4 , two layer of a part of substrate **** (GaN layer 102b) carried out longitudinal direction growth, and the big cavity was made in the side of trough, i.e., height, 101a. In addition, the TMG speed of supply at this time is 40micromol / min in general. It was a grade and th rate of crystal growth of two layer of substrate **** (GaN layer 102b) was about about 1 micrometer/Hr.
[0054] (d) According to the hydride vapor growth (the HVPE method), the crystal growth of the above-mentioned GaN layer (two layer of substrate ****) 102b was further carried out to 200 micrometers after that. The rate of crystal growth of GaN layer 102b in this HVPE method was about about 45 micrometer/Hr.
[0055] [3] Partition stage (a) The ground substrate 101 and the substrate (it consists of AlGaN buffer-layer 102a and GaN layer 102b) layer 102 were cooled to abbreviation ordinary temperature after the above-mentioned crystal-growth process, passing ammonia (NH3) gas to the reaction chamber of crystal-growth equipment. The cooling rate at this time was the "-50 degree-C/min--5 degree C/min" grade in general.
[0056] (b) When these were taken out from the reaction chamber of crystal-growth equipment after that, the GaN crystal which exfoliated from the ground substrate 101 was obtained. However, this crystal was a thing [that some / small / wreckage of AlGaN buffer-layer 102a and the fracture wreckage of height 101a have remained at the rear face of GaN layer 102b].
[0057] [4] The fracture wreckage of height 101a which consists of Si which remained in the rear face of a GaN crystal by etching processing using the mixed liquor which added the nitric acid to fluoric acid was removed after the partition stage of the fracture wreckage removal process above.
[0058] By the above manufacture method, the semiconductor substrate of the good GaN crystal of the crystallinity of about 200 micrometers of thickness which was very excellent (GaN layer 102b), i.e., the

request which became independent of the ground substrate 101, was able to be obtained.
[0059] In addition, although the height and trough of a ground substrate are constituted from an above mentioned example by a vertical plane and the level surface as illustrated to drawing 2 , you may form these from arbitrary slant faces, curved surfaces, etc. Therefore, the cross-section configuration of th trough formed on the ground substrate illustrated to drawing 2 (c) may be formed in the form of for example, the abbreviation type for U characters, the abbreviation typ for V characters, etc. besides tl **** type of an abbreviation rectangle, and, generally these configurations, a size, an interval, arrangement, orientation, etc. are arbitrary.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The typical perspective diagram of a partial fragment of the ground substrate explaining an operation of this invention which has a height, and the semiconducting crystal which grew on it.
[Drawing 2] The typical perspective diagram (a) of the partial fragment of the ground substrate (Si substrate) 101 concerning the example of this invention, a plan (b), and a cross section (c).
[Drawing 3] The typical perspective diagram (a) of the ground substrate 101 by which one layer (AlGaN buffer layer) 102of substrate **** a was formed, a plan (b), and a cross section (c).
[Drawing 4] The typical perspective diagram (a) of the ground substrate 101 to which the laminating of the substrate layer 102 (layer 102a and layer 102b) was carried out, a plan (b), and a cross section (c).
[Drawing 5] The typical cross section of the semiconducting crystal on the conventional ground substrate.
[Description of Notations]
101 -- Ground Substrate (Si Substrate)
101a -- Height
102 -- Substrate Layer (Nitride Semiconductor Layer)
102a -- One layer (AlGaN buffer layer) of substrate ****
102b -- Two layer (GaN single crystal layer) of substrate ****

[Translation done.]

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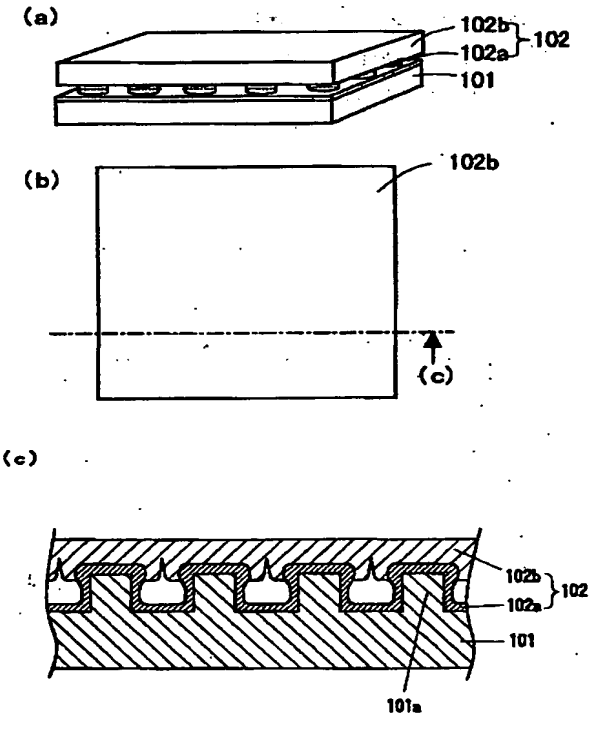
最終頁に続く

(54)【発明の名称】　半導体結晶の製造方法及び半導体発光素子

(57)【要約】
【課題】　転位の少ない高品質の半導体結晶を得る。
【解決手段】　多数の突起部を有する下地基板上にIII族窒化物系化合物より成る基板層（所望の半導体結晶）を成長させた場合、突起部の大きさや配置間隔や結晶成長諸条件等によっては、各突起部間に半導体結晶が積層されていない空洞が形成される。このため、突起部の高さに比して基板層の厚さを十分に大きくすれば、内部応力または外部応力がこの突起部に集中的に作用し易くなる。その結果、特にこれらの応力は、突起部に対する剪断応力等として作用し、この応力が大きくなった時に、突起部が破断する。従って、この応力を利用すれば、容易に下地基板と基板層とを分離することが可能となり、下地基板から独立した半導体結晶を得ることができる。空洞が大きく形成される程、突起部に上記の応力が集中し易くなり、下地基板と基板層とをより確実に分離することができる。



【特許請求の範囲】

【請求項１】　横方向結晶成長作用を利用して、下地基板上に III族窒化物系化合物半導体から成る基板層を形成することにより、前記下地基板から独立した半導体結晶を得る方法であって、

前記下地基板上に多数の突起部を形成する突起部形成工程と、

前記突起部の表面の少なくとも一部を前記基板層が結晶成長を開始する最初の成長面として、この成長面が各々互いに連結されて少なくとも一連の略平面に成長するまで、前記基板層を結晶成長させる結晶成長工程と、

前記突起部を破断することにより、前記基板層と前記下地基板とを分離する分離工程とを有することを特徴とする半導体結晶の製造方法。

【請求項２】　前記基板層と前記下地基板とを冷却または加熱することにより、前記基板層と前記下地基板との熱膨張係数差に基づく応力を発生させ、この応力を利用して前記突起部を破断することを特徴とする請求項１に記載の半導体結晶の製造方法。

【請求項３】　横方向結晶成長作用を利用して、下地基板上に III族窒化物系化合物半導体から成る基板層を形成することにより、半導体結晶を得る方法であって、

前記下地基板上に多数の突起部を形成する突起部形成工程と、

前記突起部の表面の少なくとも一部を前記基板層が結晶成長を開始する最初の成長面として、この成長面が各々互いに連結されて少なくとも一連の略平面に成長するまで、前記基板層を結晶成長させる結晶成長工程とを有し、

前記結晶成長工程において、前記 III族窒化物系化合物半導体の原料供給量ｑを調整することにより、

前記下地基板の前記突起部間の谷部の少なくとも一部の露出領域における前記III族窒化物系化合物半導体の結晶成長速度ａと、前記突起部の頭頂部における結晶成長速度ｂとの差分（ｂ－ａ）を略最大値に制御することを特徴とする半導体結晶の製造方法。

【請求項４】　前記結晶成長工程において、前記 III族窒化物系化合物半導体の原料供給量ｑを調整することにより、

前記下地基板の前記突起部間の谷部の少なくとも一部の露出領域における前記III族窒化物系化合物半導体の結晶成長速度ａと、前記突起部の頭頂部における結晶成長速度ｂとの差分（ｂ－ａ）を略最大値に制御することを特徴とする請求項１、または請求項２に記載の半導体結晶の製造方法。

【請求項５】　前記原料供給量ｑを１μmol ／min 以上、１００μmol ／min 以下としたことを特徴とする請求項３、または請求項４に記載の半導体結晶の製造方法。

【請求項６】　前記下地基板の材料として、シリコン（Ｓｉ）または炭化シリコン（ＳｉＣ）を用いることを特徴とする請求項１乃至請求項５の何れか１項に記載の半導体結晶の製造方法。

【請求項７】　前記下地基板の材料として、Ｓｉ（１１１）を用い、

前記突起部形成工程において、前記下地基板の前記突起部間の谷部の露出領域に、Ｓｉ（１１１）面が露出しない様に前記突起部を形成することを特徴とする請求項１乃至請求項６の何れか１項に記載の半導体結晶の製造方法。

【請求項８】　前記突起部形成工程後、

少なくとも前記突起部の表面に「$Al_xGa_{1-x}N$（０＜ｘ≦１）」より成るバッファ層を形成する工程を有することを特徴とする請求項１乃至請求項７の何れか１項に記載の半導体結晶の製造方法。

【請求項９】　前記バッファ層の膜厚を前記突起部の縦方向の高さ以下に成膜することを特徴とする請求項８に記載の半導体結晶の製造方法。

【請求項１０】　前記結晶成長工程において、

前記基板層の膜厚を５０μm以上としたことを特徴とする請求項１乃至請求項９の何れか１項に記載の半導体結晶の製造方法。

【請求項１１】　前記結晶成長工程において、

結晶成長速度の遅い結晶成長法から、結晶成長速度の速い結晶成長法に、途中で結晶成長法を変更することを特徴とする請求項１乃至請求項１０の何れか１項に記載の半導体結晶の製造方法。

【請求項１２】　前記突起部形成工程において、

前記突起部が略等間隔または略一定周期で配置される様に前記突起部を形成することを特徴とする請求項１乃至請求項１１の何れか１項に記載の半導体結晶の製造方法。

【請求項１３】　前記突起部形成工程において、

１辺が0.１μm以上の略正三角形を基調とする２次元三角格子の格子点上に前記突起部を形成することを特徴とする請求項１２に記載の半導体結晶の製造方法。

【請求項１４】　前記突起部形成工程において、前記突起部の水平断面形状を、略正三角形、略正六角形、略円形、又は四角形に形成したことを特徴とする請求項１乃至請求項１３の何れか１項に記載の半導体結晶の製造方法。

【請求項１５】　前記突起部形成工程において、前記突起部の配置間隔を0.１μm以上、１０μm以下とすることを特徴とする請求項１乃至請求項１４の何れか１項に記載の半導体結晶の製造方法。

【請求項１６】　前記突起部形成工程において、前記突起部の縦方向の高さを0.５μm以上、２０μm以下とすることを特徴とする請求項１乃至請求項１５の何れか１項に記載の半導体結晶の製造方法。

【請求項１７】　前記突起部形成工程において、前記突

起部の横方向の太さ、幅、又は直径を0.1μm以上、10μm以下とすることを特徴とする請求項1乃至請求項16の何れか1項に記載の半導体結晶の製造方法。

【請求項18】 前記結晶成長工程よりも前に、
各種エッチング、電子線照射処理、レーザ等の光学的処理、化学的処理、或いは切削や研磨等の物理的処理により、
前記下地基板の前記突起部間の谷部の少なくとも一部の露出領域の結晶性又は分子構造を劣化又は変化させることにより、前記露出領域における前記 III族窒化物系化合物半導体の結晶成長速度aを低下させることを特徴とする請求項1乃至請求項17の何れか1項に記載の半導体結晶の製造方法。

【請求項19】 前記分離工程において、
前記下地基板と前記基板層とから成る基板を成長装置の反応室に残し、略一定流量のアンモニア (NH_3) ガスを前記反応室に流したままの状態で、
前記基板を概ね「-100℃/min～-0.5℃/min」程度の冷却速度で略常温まで冷却することを特徴とする請求項1又は請求項2、或いは、請求項4乃至請求項18の何れか1項に記載の半導体結晶の製造方法。

【請求項20】 少なくとも前記分離工程よりも後に、前記基板層の裏面に残った前記突起部の破断残骸をエッチング等の、化学的或いは物理的な加工処理により除去する残骸除去工程を有することを特徴とする請求項1又は請求項2、或いは、請求項4乃至請求項19の何れか1項に記載の半導体結晶の製造方法。

【請求項21】 請求項1乃至請求項20の何れか1項に記載の半導体結晶の製造方法を用いて製造された、前記半導体結晶を結晶成長基板として有することを特徴とする III族窒化物系化合物半導体発光素子。

【請求項22】 請求項1乃至請求項20の何れか1項に記載の半導体結晶の製造方法を用いて製造された、前記半導体結晶を結晶成長基板とした結晶成長により製造されたことを特徴とする III族窒化物系化合物半導体発光素子。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明は、横方向結晶成長作用を利用して、下地基板上に III族窒化物系化合物半導体から成る基板層を形成することにより結晶成長基板を得る、半導体結晶の製造方法に関する。

【0002】

【従来の技術】図5に例示する様に、例えばシリコン（Si）等から成る下地基板上に窒化ガリウム（GaN）等の窒化物半導体を結晶成長させ、その後常温まで冷却すると、窒化物半導体層に転位やクラックが多数入ることが一般に知られている。

【0003】

【発明が解決しようとする課題】この様に、成長層（窒化物半導体層）に転位やクラックが多数入ると、その上にデバイスを作製した場合に、デバイス中に格子欠陥や転位、変形、クラック等が多数生じる結果となり、デバイス特性の劣化を引き起こす原因となる。また、例えばシリコン（Si）等から成る下地基板を除去し、成長層のみを残して、独立した基板（結晶）を得ようとする場合、上記の転位やクラック等の作用により、大面積（1 cm^2 以上）のものが得られない。

【0004】本発明は、上記の課題を解決するために成されたものであり、その目的は、クラックが無く、転位の密度が低い高品質の半導体結晶（結晶成長基板）を得ることである。

【0005】

【課題を解決するための手段、並びに、作用及び発明の効果】上記の課題を解決するためには、以下の手段が有効である。即ち、第1の手段は、横方向結晶成長作用を利用して下地基板上に III族窒化物系化合物半導体から成る基板層を形成することにより下地基板から独立した半導体結晶を得る製造工程において、下地基板上に多数の突起部を形成する突起部形成工程と、この突起部の表面の少なくとも一部を基板層が結晶成長を開始する最初の成長面としてこの成長面が各々互いに連結されて少なくとも一連の略平面に成長するまで基板層を結晶成長させる結晶成長工程と、突起部を破断することにより基板層と下地基板とを分離する分離工程とを設けることである。

【0006】ただし、ここで言う「 III族窒化物系化合物半導体」一般には、2元、3元、又は4元の「$Al_xGa_yIn_{(1-x-y)}N$（$0 \leqq x \leqq 1$，$0 \leqq y \leqq 1$，$0 \leqq x+y \leqq 1$）」成る一般式で表される任意の混晶比の半導体が含まれ、更に、p型或いはn型の不純物が添加された半導体も、本明細書の「 III族窒化物系化合物半導体」の範疇とする。また、上記の III族元素（Al，Ga，In）の内の一部をボロン（B）やタリウム（Tl）等で置換したり、或いは、窒素（N）の一部をリン（P）、砒素（As）、アンチモン（Sb）、ビスマス（Bi）等で置換したりした半導体等もまた、本明細書の「 III族窒化物系化合物半導体」の範疇とする。また、上記のp型の不純物としては、例えば、マグネシウム（Mg）や、或いはカルシウム（Ca）等を添加することができる。また、上記のn型の不純物としては、例えば、シリコン（Si）や、硫黄（S）、セレン（Se）、テルル（Te）、或いはゲルマニウム（Ge）等を添加することができる。また、これらの不純物は、同時に2元素以上を添加しても良いし、同時に両型（p型とn型）を添加しても良い。

【0007】例えば、図1に例示する様に、多数の突起部を有する下地基板上に III族窒化物系化合物より成る基板層（半導体結晶）を成長させる場合、突起部の大きさや配置間隔や結晶成長諸条件等を調整することによ

り、各突起部間（突起部の側方）に、半導体結晶が積層されていない「空洞」が形成可能となる。このため、突起部の高さに比して基板層の厚さを十分に大きくすれば、内部応力または外部応力がこの突起部に集中的に作用し易くなる。その結果、特にこれらの応力は、突起部に対する剪断応力等として作用し、この応力が大きくなった時に、突起部が破断する。従って、この応力を利用すれば、容易に下地基板と基板層とを分離（剥離）することが可能となる。この手段により、下地基板から独立した結晶（基板層）を得ることができる。また、上記の「空洞」が大きく形成される程、突起部に応力（剪断応力）が集中し易くなる。

【０００８】また、例えば、図１からも分かる様に、上記の様な突起部を形成することにより、下地基板と基板層（又は、所望の半導体結晶層）との接触部位が狭く限定されるため、両者の格子定数差に基づく歪が生じ難くなり、「下地基板と基板層の間の格子定数差に基づく応力」が緩和される。このため、基板層（所望の半導体結晶）が結晶成長する際に、成長中の基板層に働く不要な応力が抑制されて転位やクラックの発生密度が低減される。

【０００９】尚、下地基板と基板層とを分離（剥離）する際に、下地基板側に基板層の一部が残っても良いし、或いは、基板層側に下地基板の一部（例：突起部の破断残骸）が残っても良い。即ち、上記の分離工程は、これらの材料の一部の残骸を皆無とする様な各材料の完全な分離を前提（必要条件）とするものではない。

【００１０】また、上記の課題を解決する第２の手段は、これらの第１の手段において、基板層と下地基板とを冷却または加熱することにより、基板層と下地基板との熱膨張係数差に基づく応力を発生させ、この応力を利用して上記の突起部の破断を実施することである。この手段によれば、上記の応力を容易に生成することが可能となる。

【００１１】また、第３の手段は、横方向結晶成長作用を利用して下地基板上にIII族窒化物系化合物半導体から成る基板層を形成することにより半導体結晶を得る製造工程において、下地基板上に多数の突起部を形成する突起部形成工程と、この突起部の表面の少なくとも一部を基板層が結晶成長を開始する最初の成長面としてこの成長面が各々互いに連結されて少なくとも一連の略平面に成長するまで基板層を結晶成長させる結晶成長工程とを設け、この結晶成長工程においてIII族窒化物系化合物半導体の原料供給量ｑを調整することにより、下地基板の突起部間の谷部の少なくとも一部の露出領域におけるIII族窒化物系化合物半導体の結晶成長速度ａと、突起部の頭頂部における結晶成長速度ｂとの差分（ｂ－ａ）を略最大値に制御することである。

【００１２】この手段によれば、突起部の頭頂部付近の結晶成長速度が相対的に大きくなり、上記の露出領域付近の結晶成長は比較的抑制されて、頭頂部付近からの結晶成長が支配的となる。この結果、突起部の頭頂部付近から開始される基板層の横方向成長（ＥＬＯ）が顕著となり、基板層の結晶成長時に基板層に働く「下地基板と基板層の間の格子定数差に基づく応力」が緩和される。従って、基板層の結晶構造が安定し、基板層に転位やクラックが発生し難くなる。また、基板層の横方向成長（ＥＬＯ）が顕著となれば、例えば、突起部の側方（各突起部間）に比較的大きな空洞ができる場合もある。

【００１３】例えば、図１に例示する様に、適当な大きさ、間隔、或いは周期で下地基板の表面上に凹凸を形成した場合、一般に、下地基板の外周側壁付近の周辺部分以外では、凸部（突起部）の上面付近に比べて、凹部（谷部）の方が結晶材料の単位時間・単位面積当たりの供給量は少なくなり易い。この傾向は、結晶材料のガス流の流量、温度、方向等にも依存するが、これらの諸条件を最適、或いは好適に制御することにより、上記の差分（ｂ－ａ）を略最大値に制御することが可能となる。

【００１４】また、第４の手段は、上記の第１または第２の手段の結晶成長工程において、III族窒化物系化合物半導体の原料供給量ｑを調整することにより、下地基板の突起部間の谷部の少なくとも一部の露出領域におけるIII族窒化物系化合物半導体の結晶成長速度ａと、突起部の頭頂部における結晶成長速度ｂとの差分（ｂ－ａ）を略最大値に制御することである。

【００１５】この場合にも、上記の手段と同様に、基板層の結晶成長時に基板層に働く「下地基板と基板層の間の格子定数差に基づく応力」が緩和され、基板層の結晶構造が安定し、基板層に転位やクラックが発生し難くなる。この作用・効果は、各突起部間（突起部の側方）に空洞ができる程に横方向成長が顕著な場合に、比較的顕著となる。また、突起部の側方（各突起部間）に空洞が形成されれば、突起部に剪断応力が集中し易くなり、上記の分離工程において下地基板と基板層とを剪断応力により分離し易くなる。この作用・効果は、各突起部間（突起部の側方）の空洞が大きくなる程、顕著となる。

【００１６】また、第５の手段は、上記の第３または第４の手段において、上記の原料供給量ｑを１μmol／min 以上、１００μmol／min 以下とすることである。

【００１７】より望ましくは、上記の原料供給量ｑは、５μmol／min 以上、９０μmol／min 以下が良い。更に望ましい値としては、形成される突起部の大きさや形、配置間隔等の下地基板の仕様や、供給原料の種類や供給流方向、結晶成長法等の諸条件にも依るが、概ね１０～８０μmol／min 程度が理想的である。この値は、大き過ぎると上記の差分（ｂ－ａ）を略最大値に制御することが難しくなるので、各突起部間（突起部の側方）に大きな空洞を形成することが難しくなる。従って、この様な場合には、格子定数差に基づく結晶内の応力が比較的緩和され難く、転位が発生する等、基板層の単結晶

の結晶性が劣化し易くなってしまい望ましくない。

【００１８】また、応力（剪断応力）により、下地基板と基板層とを分離する際にも、突起部側方の空洞が無いか或いはこの空洞が小さいと、突起部に応力が集中し難くなり、突起部の破断が起り難くなってしまい望ましくない。一方、原料供給量qが小さ過ぎると、結晶成長時間が掛かり過ぎて生産性の面で不利となり、望ましくない。

【００１９】また、第６の手段は、上記の第１乃至第５の何れか１つの手段において、下地基板の材料として、シリコン（Ｓｉ）または炭化シリコン（ＳｉＣ）を用いることである。また、その他の下地基板の材料としては、例えば、ＧａＮ，ＡｌＮ，ＧａＡｓ，ＩｎＰ，ＧａＰ，ＭｇＯ，ＺｎＯ，$MgAl_2O_4$ 等が有用で、また、サファイア、スピネル、酸化マンガン、酸化ガリウムリチウム（$LiGaO_2$）、硫化モリブデン（ＭｏＳ）等も使用可能である。ただし、熱膨張係数差に基づく剪断応力を用いて下地基板と基板層とを分離する場合には、両材料間の熱膨張係数差が小さくならない組み合わせを選択することが望ましく、また、下地基板側には、破断が起り易い材料を選択することが望ましい。

【００２０】また、第７の手段は、上記の第１乃至第６の何れか１つの手段において、下地基板の材料としてＳｉ（１１１）を用い、突起部形成工程において下地基板の突起部間の谷部の露出領域にＳｉ（１１１）面が露出しない様に突起部を形成することである。本手段によれば、上記の谷部の露出面の結晶成長速度ａを小さく抑制できるため、上記の差分（ｂ－ａ）を、結晶性を維持したまま安定的に略最大化することが可能となる。

【００２１】また、第８の手段は、上記の第１乃至第７の何れか１つの手段の突起部形成工程後に、少なくとも突起部の表面に「$Al_xGa_{1-x}N$（０＜ｘ≦１）」より成るバッファ層を形成する工程を設けることである。

【００２２】ただし、上記のバッファ層とは別に、更に、上記のバッファ層と略同組成（例：ＡｌＮや、ＡｌＧａＮ）の中間層を周期的に、又は他の層と交互に、或いは、多層構造が構成される様に、積層しても良い。

【００２３】この様なバッファ層（或いは、中間層）の積層により、格子定数差に起因する基板層（成長層）に働く応力を緩和できる等の従来と同様の作用原理により、結晶性を向上させることが可能となる。

【００２４】また、第９の手段は、上記の第８の手段において、バッファ層の膜厚を突起部の縦方向の高さ以下に成膜することである。また、絶対的な目安としては、バッファ層の膜厚は、およそ0.０１μｍ以上、１μｍ以下が望ましい。この手段により、バッファ層の上に形成される所望の結晶層（例：ＧａＮ層）のみを良質に横方向に成長させることができる。即ち、この手段により、バッファ層の上に形成される結晶層に結晶成長時に掛かる「格子定数差に基づく応力」が軽減され、転位密度が効果的に低減できる。

【００２５】バッファ層等を形成するＡｌＮやＡｌＧａＮ等は、下地基板の露出した表面の略全面に成膜され易く、また、元来、所望の結晶の成長層等を形成するＧａＮの方が、ＡｌＮやＡｌＧａＮ等よりも横方向成長し易い傾向に有る様だが、上記の手段によれば、より確実に大きな「空洞」を突起部の側方に形成することができる。

【００２６】また、この手段により、基板層を下地基板から分離した際に、基板層の裏面（下地基板が有った側の面）にも、結晶層（バッファ層の上に形成される所望の層）が直に広範囲に露出する。従って、基板層の裏面に電極を形成する際に、電気抵抗を抑制することが容易となる。

【００２７】尚、バッファ層の膜厚は、上記の通りおよそ0.０１μｍ～１μｍ程度が概ね妥当な範囲であるが、より望ましくは、0.１μｍ以上、0.５μｍ以下が良い。この膜厚が厚過ぎると、空洞が小さくなり易くなり望ましくない。また、この膜厚を薄くし過ぎると、略均一にバッファ層を成膜することが困難となる。特に、突起部の上部付近においてバッファ層の成膜ムラ（十分に成膜されない部位）が生じると、結晶性にもムラが生じ易くなり、望ましくない。

【００２８】また、第１０の手段は、上記の第１乃至第９の何れか１つの手段の結晶成長工程において、基板層の膜厚を５０μｍ以上とすることである。

【００２９】結晶成長させる基板層（ III族窒化物系化合物半導体）の厚さは、約５０μｍ以上が望ましく、この厚さが厚い程、基板層に対する引っ張り応力が緩和されて、基板層の転位やクラックの発生密度を減少できる。また、更には、同時に基板層を強固にでき、上記の剪断応力を上記の突起部に集中させ易くなる。

【００３０】また、第１１の手段は、上記の第１乃至第１０の何れか１つの手段の結晶成長工程において、結晶成長速度の遅い結晶成長法から、結晶成長速度の速い結晶成長法に、途中で結晶成長法を変更することである。

【００３１】例えば、結晶成長面が一連の略平面状に成るまでは、上記の差分（ｂ－ａ）を略最大にし易い結晶成長法（例：ＭＯＶＰＥ法）を採用し、その後は、膜厚を効率よく５０μｍ以上にすることが容易な結晶成長法（例：ＨＶＰＥ法）を採用すれば、短時間に結晶性の良質な半導体結晶を得ることが可能となる。

【００３２】また、第１２の手段は、上記の第１乃至第１１の何れか１つの手段の突起部形成工程において、突起部が略等間隔又は略一定周期で配置される様に上記の突起部を形成することである。

【００３３】これにより、横方向成長の成長条件が全体的に略均等となり、結晶性の良否にムラが生じ難くなる。また、突起部間の谷部の上方が、基板層によって完全に覆われるまでの時間に、局所的なバラツキが生じ難

くなるため、例えば、結晶成長速度の遅い結晶成長法から、結晶成長速度の速い結晶成長法に、途中で結晶成長法を変更する場合に、その時期を的確に、早期に、或いは一意に決定することが容易となる。また、本手段により、上記の空洞が各々略均等な大きさとなり、上記の剪断応力を各突起部に略均等に分配することが可能となるため、全突起部の破断がムラなく生じ、下地基板と基板層との分離が確実に実施できる様になる。

【００３４】また、第１３の手段は、上記の第１２の手段の突起部形成工程において、１辺が0.１μm以上の略正三角形を基調とする２次元三角格子の格子点上に突起部を形成することである。この手段により、上記の第１２の手段をより具体的に正確、確実に実施でき、よって、転位の数を確実に低減することができる。

【００３５】また、第１４の手段は、上記の第１乃至第１３の何れか１つの手段の突起部形成工程において、突起部の水平断面形状を、略正三角形、略正六角形、略円形、又は四角形に形成することである。この手段により、III族窒化物系化合物半導体より形成される結晶の結晶軸の方向が各部で揃い易くなるため、或いは、任意の水平方向に対して突起部の水平方向の長さ（太さ）を略一様に制限できるため、転位の数を抑制することができる。特に、正六角形や正三角形は、半導体結晶の結晶構造と合致し易いのでより望ましい。また、円形や四角形は製造技術の面で形成し易いと言う、現行一般の加工技術水準の現状に照らしたメリットが有る。

【００３６】また、第１５の手段は、上記の第１乃至第１４の何れか１つの手段の突起部形成工程において、突起部の配置間隔（配置周期）を0.１μm以上、１０μm以下とすることである。より望ましくは、結晶成長の実施条件にも依存するが、突起部の配置間隔は、0.５～８μm程度が良い。ただし、この配置間隔とは、互いに接近する各突起部の中心点間の距離のことを言う。

【００３７】この手段により、突起部の谷部の上方を基板層で覆うことが可能となると同時に、突起部間に空洞を形成することが可能となる。この値が小さ過ぎると、ＥＬＯの作用が殆ど得られなくなり、結晶性が劣化する。また、形成される空洞が小さくなり過ぎて、基板層の膜厚を必要以上に大きくしない限り、突起部を破断することが容易でなくなる。

【００３８】また、この値が大きくなり過ぎると、確実に突起部の谷部の上方を基板層で覆うことができなくなり、結晶性が均質かつ良質の結晶（基板層）が得られなくなる。或いは、この値が更に大き過ぎると、谷部の露出面が広大となり過ぎて、ＥＬＯの作用が殆ど得られなくなり、また、空洞が全く形成されなくなるため、結晶性が劣化し、また、基板層の膜厚を必要以上に大きくしない限り、突起部を破断することが容易でなくなる。

【００３９】また、第１６の手段は、上記の第１乃至第１５の何れか１つの手段の突起部形成工程において、突起部の縦方向の高さを0.５μm以上、２０μm以下とすることである。より望ましくは、結晶成長の実施条件にも依存するが、突起部の縦方向の高さは、0.８～５μm程度が良い。この高さが短過ぎると、突起部が無い場合と同様に、ＥＬＯの作用が殆ど得られなくなり、結晶性が劣化する。また、この高さが短過ぎると、上記の空洞が形成されなくなる。また、この高さが高過ぎると、突起部の形成自身が困難となったり、突起部の形成に必要以上に時間がかかったり、下地基板の材料が必要以上に消費されたりして望ましくない。また、この高さが高過ぎると、剪断応力が突起部の縦方向に分散されてしまい、突起部を確実に破断させることが難しくなる。

【００４０】また、第１７の手段は、上記の第１乃至第１６の何れか１つの手段の突起部形成工程において、突起部の横方向の太さ、幅、又は直径を0.１μm以上、１０μm以下とすることである。より望ましくは、結晶成長の実施条件にも依存するが、突起部の横方向の太さ、幅、又は直径は、0.５～５μm程度が良い。この太さが太過ぎると、格子定数差に基づいて基板層（成長層）に働く応力の影響が大きくなり、基板層の転位数が増加し易くなる。また、細過ぎると、突起部自身の形成が困難となるか、或いは、突起部の頭頂部の結晶成長速度bが遅くなり、望ましくない。

【００４１】また、応力（剪断応力等）により突起部を破断させる際にも、突起部の横方向の太さ、幅、又は直径が大き過ぎると、確実に破断されない部分が生じ易くなり、望ましくない。また、格子定数差に基づいて基板層（成長層）に働く応力の影響の大小は、突起部の横方向の太さ（長さ）だけに依るものではなく、突起部の配置間隔等にも依存する。そして、これらの設定範囲が不適切であれば、上記の様に格子定数差に基づく応力の影響が大きくなり、基板層の転位数が増加し易くなり、望ましくない。

【００４２】また、突起部の頭頂部付近の横方向の太さ、幅、又は直径には、上記の様に最適値又は適正範囲があるため、突起部の上面、底面、又は水平断面の形状は、少なくとも局所的に閉じた形状（島状）、更には、外側に向かって凸状に閉じた形状が良く、より望ましくは、この上面、底面、又は水平断面の形状は、略円形や略正多角形等が良い。この様な設定により、任意の水平方向に対して確実に、上記の最適値又は適正範囲を実現することが容易となる。

【００４３】また、第１８の手段は、上記の第１乃至第１７の何れか１つの手段において、結晶成長工程よりも前に、各種エッチング、電子線照射処理、レーザ等の光学的処理、化学的処理、或いは切削や研磨等の物理的処理により、下地基板の突起部間の谷部の少なくとも一部の露出領域の結晶性又は分子構造を劣化又は変化させることにより、この露出領域におけるIII族窒化物系化合物半導体の結晶成長速度aを低下させることである。こ

の手段により、前記の結晶成長速度の差分（ｂ－ａ）をより大きくすることができる。従って、この手段によれば、突起部の頭頂部付近の結晶成長速度が相対的に大きくなるため、前記と同様の作用により、基板層の結晶成長時に基板層に働く「下地基板と基板層の間の格子定数差に基づく応力」が緩和され、基板層に転位やクラックが発生し難くなる。

【００４４】また、第１９の手段は、上記の何れか１つの分離工程において、下地基板と基板層とから成る基板を成長装置の反応室に残し、略一定流量のアンモニア（NH_3）ガスを反応室に流したままの状態で、基板を概ね「－１００℃／ｍｉｎ～－0.5℃／ｍｉｎ」程度の冷却速度で略常温まで冷却することである。例えば、この様な手段により、基板層の結晶性を良質に維持したまま、前記の分離工程を実施することができる。

【００４５】また、第２０の手段は、少なくとも、上記の何れか１つの分離工程よりも後に、基板層の裏面に残った突起部の破断残骸をエッチング等の、化学的或いは物理的な加工処理により除去する残骸除去工程を設けることである。この手段によれば、基板層の裏面（下地基板を剥離させた側の面）に、半導体発光素子等の電極を形成した際に、電極と基板層との界面付近に生じる電流ムラや電気抵抗を抑制でき、よって駆動電圧の低減や、或いは発光強度の向上等を図ることができる。

【００４６】更に、突起部の破断残骸を除去することにより、電極を半導体発光素子等の反射鏡としても利用する際には、鏡面付近での光の吸収や散乱が低減されて反射率が向上するので、発光強度が向上する。また、例えば、研磨等の物理的な加工処理によりこの残骸除去工程を実施した場合等には、基板層の裏面のバッファ層までをも取り除いたり、或いは、基板層の裏面の平坦度を向上したりすることもできるので、電流ムラや電気抵抗の抑制、或いは、鏡面付近での光の吸収や散乱の低減等の、上記の作用効果を更に補強することができる。

【００４７】また、第２１の手段は、III族窒化物系化合物半導体発光素子において、上記の第１乃至第２０の何れか１つの手段に依る半導体結晶の製造方法を用いて製造された半導体結晶を結晶成長基板として備えることである。この手段によれば、結晶性が良質で、内部応力の少ない半導体より、III族窒化物系化合物半導体発光素子を製造することが可能又は容易となる。

【００４８】また、第２２の手段は、上記の第１乃至第２０の何れか１つの手段に依る半導体結晶の製造方法を用いて製造された半導体結晶を結晶成長基板とした結晶成長により、III族窒化物系化合物半導体発光素子を製造することである。この手段によれば、結晶性が良質で、内部応力の少ない半導体より、III族窒化物系化合物半導体発光素子を製造することが可能又は容易となる。以上の手段により、前記の課題を解決することができる。

【００４９】

【発明の実施の形態】以下、本発明を具体的な実施例に基づいて説明する。ただし、本発明は以下に示す実施例に限定されるものではない。以下、本発明の実施例における半導体結晶（結晶成長基板）の製造手順の概要を例示する。

【００５０】〔１〕突起部形成工程

図２に示す様に、シリコンより成る単結晶の下地基板１０１のＳｉ（１１１）面上に、フォトリソグラフィーを利用したドライエッチングにより、直径約１μｍ、高さ約１μｍの略円柱形状の突起部１０１ａを約２μｍの配置間隔で形成した。配列形態としては、一辺が約２μｍの略正三角形を基調とする２次元三角格子の各格子点上に突起部１０１ａの円柱底面の中心が配置される様に、突起部１０１ａを形成した。ただし、下地基板１０１の厚さは約２００μｍとした。

【００５１】〔２〕結晶成長工程

本結晶成長工程では、図４に示す様に、結晶の成長面が、突起部１０１ａの上面（初期状態）から各々互いに連結されて一連の略平面状に成長するまでの成長工程を有機金属化合物気相成長法（ＭＯＶＰＥ法）に従って実施し、その後、この基板層（結晶層）が２００μｍ程度の厚膜に成長するまでの成長工程をハイドライド気相成長法（ＨＶＰＥ法）に従って実施した。尚、本結晶成長工程では、アンモニア(NH_3) ガス、キャリアガス(H_2, N_2) 、トリメチルガリウム($Ga(CH_3)_3$)ガス（以下「TMG」と記す）、及びトリメチルアルミニウム($Al(CH_3)_3$) ガス（以下「TMA 」と記す）を用いた。

【００５２】（ａ）まず、上記の突起部１０１ａが設けられた下地基板１０１（図２）を有機洗浄及び酸処理により洗浄し、結晶成長装置の反応室に載置されたサセプタに装着し、常圧でH_2を反応室に流しながら温度1100℃で下地基板１０１をベーキングした。

【００５３】（ｂ）次に、上記の下地基板１０１の上に、ＭＯＶＰＥ法に従って、H_2 , NH_3, ＴＭＧ, ＴＭＡを供給して、ＡｌＧａＮバッファ層（基板層第１層）１０２ａを成膜した。このＡｌＧａＮバッファ層１０２ａの結晶成長温度は、約１１００℃、膜厚は約0.３μｍであった。（図３）

（ｃ）このＡｌＧａＮバッファ層（基板層第１層）１０２ａの上に、基板層第２層の一部、即ち、膜厚約５μｍのＧａＮ層１０２ｂを、H_2、NH_3 及びＴＭＧを供給して、成長温度１０７５℃で結晶成長させた。この工程により、図４に示す様に、基板層第２層（ＧａＮ層１０２ｂ）の一部が横方向成長し、谷部即ち突起部１０１ａの側方に大きな空洞ができた。尚、この時のＴＭＧ供給速度は、概ね４０μmol ／min 程度であり、基板層第２層（ＧａＮ層１０２ｂ）の結晶成長速度は、約１μｍ／Ｈｒ程度であった。

【００５４】（ｄ）その後、ハイドライド気相成長法

（ＨＶＰＥ法）に従って、上記のＧａＮ層（基板層第２層）１０２ｂを、更に、２００μｍまで結晶成長させた。このＨＶＰＥ法におけるＧａＮ層１０２ｂの結晶成長速度は、約４５μｍ／Ｈｒ程度であった。

【００５５】〔３〕分離工程

（ａ）上記の結晶成長工程の後、アンモニア（NH_3）ガスを結晶成長装置の反応室に流したまま、下地基板１０１と、（ＡｌＧａＮバッファ層１０２ａとＧａＮ層１０２ｂとから成る）基板層１０２を略常温まで冷却した。この時の冷却速度は、概ね「－５０℃／ｍｉｎ～－５℃／ｍｉｎ」程度であった。

【００５６】（ｂ）その後、これらを結晶成長装置の反応室から取り出すと、下地基板１０１から剥離したＧａＮ結晶が得られた。ただし、この結晶は、ＧａＮ層１０２ｂの裏面に、ＡｌＧａＮバッファ層１０２ａの小さな一部分の残骸と突起部１０１ａの破断残骸とが残留したままのものであった。

【００５７】〔４〕破断残骸除去工程

上記の分離工程の後、フッ酸に硝酸を加えた混合液を用いたエッチング処理により、ＧａＮ結晶の裏面に残ったＳｉより成る突起部１０１ａの破断残骸を除去した。

【００５８】以上の製造方法により、膜厚約２００μｍの結晶性の非常に優れた良質のＧａＮ結晶（ＧａＮ層１０２ｂ）、即ち、下地基板１０１から独立した所望の半導体基板を得ることができた。

【００５９】尚、上記の実施例では、図２に例示した様に、下地基板の突起部や谷部は鉛直面と水平面により構成されているが、これらは任意の斜面や曲面等から形成しても良い。従って、図２（ｃ）に例示した下地基板上に形成される谷部の断面形状は、略矩形の凹字型以外にも、例えば、略Ｕ字型や略Ｖ字型等の形に形成しても良く、一般にこれらの形状、大きさ、間隔、配置、配向等は任意である。

【図面の簡単な説明】

【図１】本発明の作用を説明する、突起部を有する下地基板と、その上に成長した半導体結晶の、部分的な断片の模式的な斜視図。

【図２】本発明の実施例に係わる、下地基板（Ｓｉ基板）１０１の部分的な断片の模式的な斜視図（ａ）、平面図（ｂ）、及び断面図（ｃ）。

【図３】基板層第１層（ＡｌＧａＮバッファ層）１０２ａが成膜された下地基板１０１の模式的な斜視図（ａ）、平面図（ｂ）、及び断面図（ｃ）。

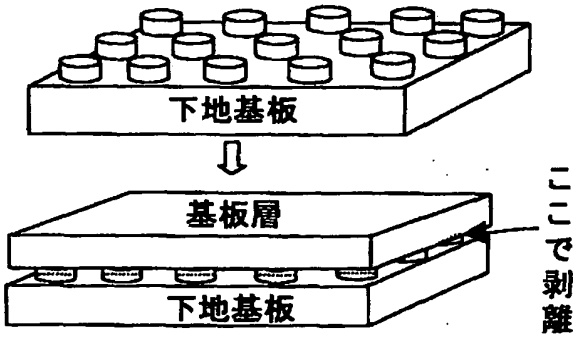
【図４】基板層１０２（層１０２ａ及び層１０２ｂ）が積層された下地基板１０１の模式的な斜視図（ａ）、平面図（ｂ）、及び断面図（ｃ）。

【図５】従来の下地基板上の半導体結晶の模式的な断面図。

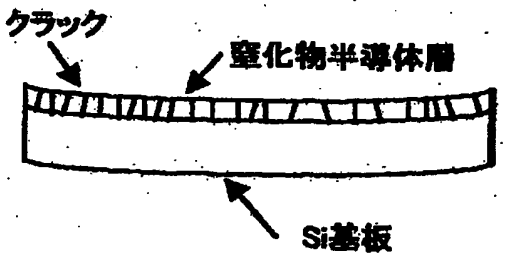
【符号の説明】

１０１　…　下地基板（Ｓｉ基板）
１０１ａ　…　突起部
１０２　…　基板層（窒化物半導体層）
１０２ａ　…　基板層第１層（ＡｌＧａＮバッファ層）
１０２ｂ　…　基板層第２層（ＧａＮ単結晶層）

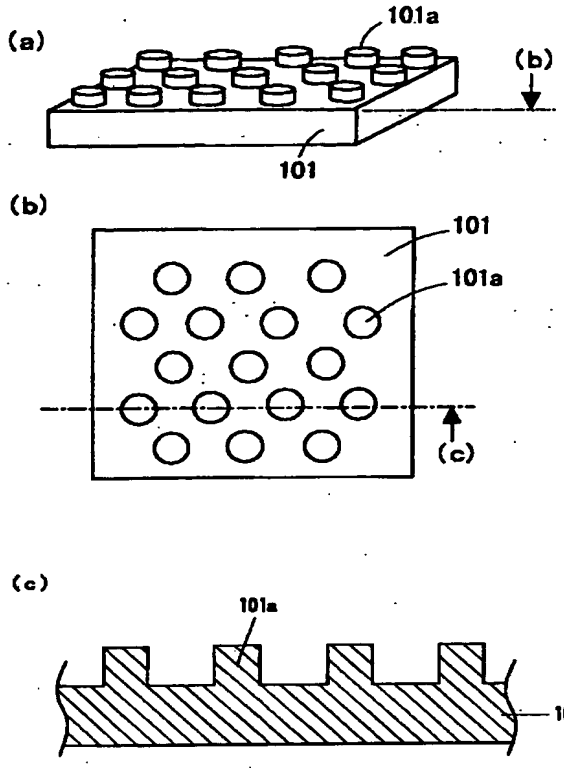
【図１】



【図５】



【図2】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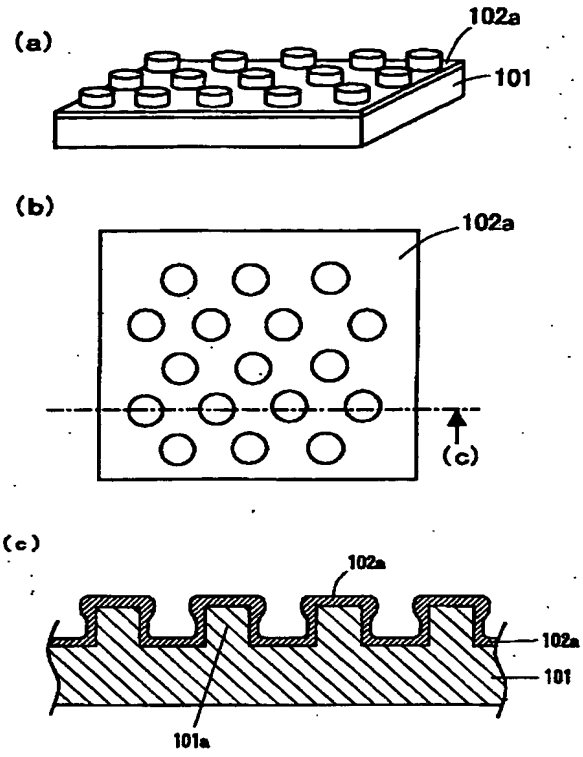
(b)
101
(b)
101
101a
(c)
(c)
101a
101

【図3】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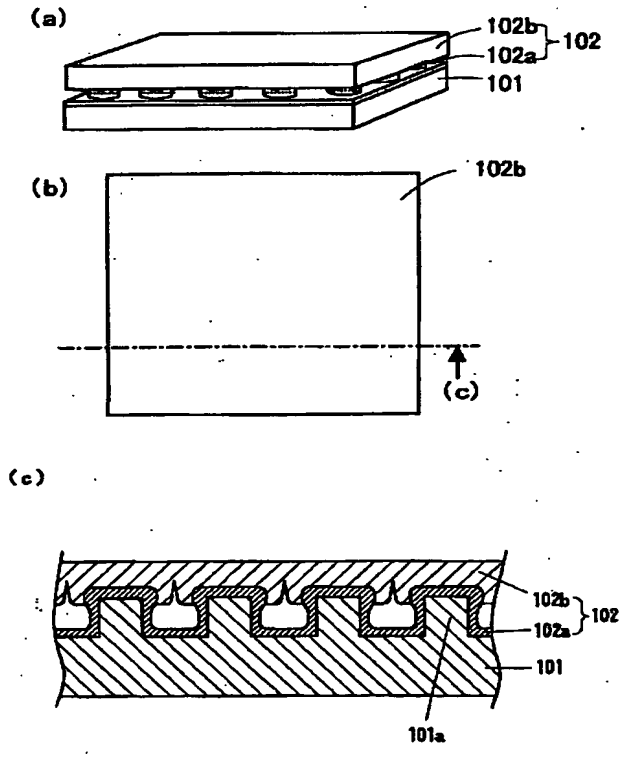
(b)
102a
(c)
(c)
102a
102a
101
101a

【図4】


(a)
102b
102a
102
101
(b)
102b
(c)
(c)
102b
102a
102
101
101a

フロントページの続き

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EF03 FJ03 TK01 TK04 TK06
TK10 TK11
5F041 AA40 CA33 CA40 CA67 CA77
5F045 AA04 AB09 AB14 AC08 AC12
AC15 AD14 AE29 AF02 AF03
BB01 BB02 BB11 BB12 BB13
CA09 CB02 DA53 EE12 HA01
HA02 HA08 HA09 HA11 HA12